Chipset for Flexible and Scalable High-Performance Gate Drivers for 1200 V - 6500 V IGBTs

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***Abstract*— The chipset presented here offers an integrated 8 A / 1 W gate driver core, direct driving of external n-type DMOS for easy scaling of the gate power and current, as well as control, monitoring and interfacing for a diversity of applications. It also features a semi-custom array containing preconfigured cells and devices to allow application-specific customization. The DMOS are driven by a regulated gate-source voltage that tracks the process and temperature variations. The chipset includes circuitry to adjust the gate-emitter voltage of the IGBT at turn-on and allow closed-loop control of the collector-emitter voltage of the IGBT at turn-off. The transformer interface transmits command and fault signals via a common channel. In case of a collision, the fault signal dominates both the command signal and noise thanks to a longer pulse duration.**

I. Introduction

Standardized integrated gate drivers are available at low cost for high-volume applications of IGBT modules up to 100 A / 1200 V and 600 A / 600 V [1]. Although dedicated gate driver ASICs may also be attractive for low-volume high-power applications due to their advanced reliability, functionality [2] and compactness [3] [4], they suffer from high development costs.

The increasingly complex and dynamic customer demands made on IGBT gate drivers, especially in the higher current and voltage ranges [5] [6] [7] [8], call for dedicated solutions to optimize performance, reliability and scalability as well as application flexibility and time-to-market at reasonable cost. Figure 1 shows the partitioning of a new flexible chipset implemented in an extended-drain CMOS foundry process (50 V double-well dual gate oxide double-metal 0.8 µm) widely used today for automotive applications. The chipset includes several variants of secondary-side gate driver ASICs and a primary-side interface ASIC. The active die area is about 4 mm x 2 mm.

The chipset is specifically optimized to fit various IGBTs and applications ranging from 150 A to 3600 A and 1200 V to 6500 V. Bonding variants are used to control the specific functionality of various standard products at very low cost. Advanced control and customer-specific options are also available through single mask-programmable preconfigured mixed-signal cells, primitive devices and routing channels (such as analog comparators, logic gates, CMOS transistors and pads) for a minimum time to market at competitive cost.

II. Implementation

The primary side ASIC of the highly integrated gate-driver core implements a dual-channel bidirectional signal transformer interface, scalable setup and fault management as well as a scalable DC-DC converter with a dedicated startup sequence and integrated output stages designed for a transferred gate power of 2 W at an ambient temperature of 85 °C in a SOIC-16 package. The secondary side ASIC includes advanced control and interfacing options and an output driver stage with a 8 A source and sink current capability at a supply voltage of up to 30 V. Both ASICs also support the direct driving of auxiliary n-type DMOS for easy scaling of the gate power and current up to 20 W, 20 A and beyond.

Whenever possible, high-voltage circuitry works with a reduced gate oxide thickness at gate-source voltages below 5.5 V to increase the transconductance per area, thereby reducing the cost and signal delay.

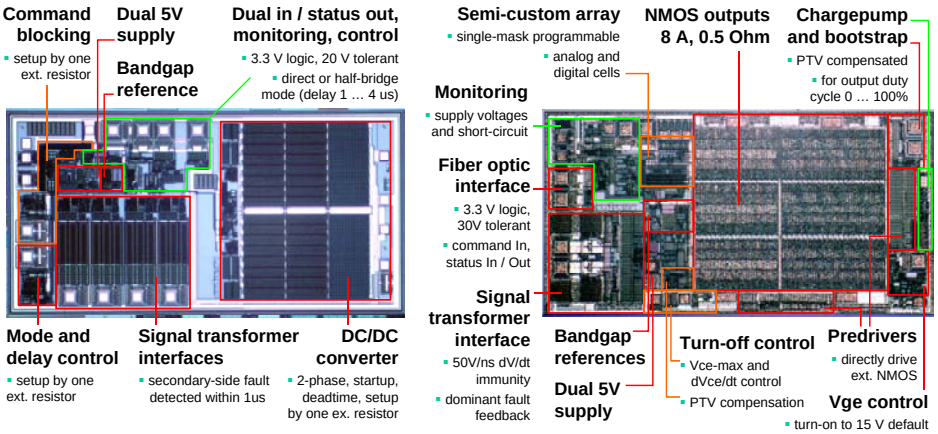

Fig. 1: Flexible and scalable IGBT driver chipset; primary-side (left) and secondary-side (right) ASICs.

Digital/power and analog circuitry works in separate fully integrated dual-output 5 V auxiliary power supplies to reduce noise and delay jitter. The timing control ranges from microseconds (e.g. for half-bridge dead time control) up to hundreds of milliseconds (e.g. for fault processing and startup sequence) and has been fully integrated by combining analog timers and asynchronous digital counters.

A. Gate Driver Output Stages

The gate driver uses lateral n-type DMOS. Their limiting factors are a high silicon cost per on-resistance and the variance of their saturation current and on-resistance over the process and temperature. The resulting timing divergences may have a severe impact on the system, e.g. on the current distribution between parallel-connected IGBTs with separate gate drivers.

These DMOS are therefore driven by a regulated gate-source voltage that tracks the process and temperature variations and also optimizes the tradeoff between performance and hot-carrier degradation. The dynamic voltage drop via the source wiring resistance is also compensated (Figure 2). For the turn-off path, the saturation current is regulated to 9.5 A ± 10 % by a gate-source voltage of between 3.8 V to 5.8 V for a temperature of between –40 °C to 150 °C. Other options are also available.

The regulated gate-source voltage for the turn-on driver DMOS is provided by combining an adaptive charge pump with a regulated constant-current bootstrap power supply for IGBT switching frequencies up to 40 kHz and 750 kHz respectively. Both are fully integrated except for one external capacitor. This enables a range of duty factors for the output pulse from 0 to 1 and also supports the direct driving of external n-type DMOS. Despite the increased complexity, this solution takes up no more silicon area than a simple p-MOS output stage.

These measures also permit accurate control of the transient and static behavior of IGBTs.

B. IGBT Turn-off Control

The ASIC also incorporates circuitry to realize closed-loop control of both the rate of rise and clamping level of the collector-emitter voltage of the IGBT at turn-off. As a result, the IGBT-internal DMOS gate channel is kept active during the full turn-off transition. A faster response, reduced turn-off switching losses and enhanced short-circuit and overcurrent turn-off capability can then be achieved.

Distributed IC device and RC-interconnect network simulation models have been used for layout optimization to achieve low wiring resistance and sufficient current distribution and to find the optimum location for the auxiliary source terminal. For an equivalent lumped model for the turn-off DMOS, the total drain-source resistance is 0.5 Ω, the source wiring resistance is 100 mΩ and the gate wiring resistance is 7.5 Ω. These parameters have been validated by measurements. The optimum closed-loop control of the IGBT turn-off transition has been determined in combination with IGBT and diode models implemented in VHDL-AMS. Medium-gain current-mode control (Figure 2) achieves fast response times in the nanosecond range. A constant current of 45 mA is subtracted from the actual input current of the control system. Up to a soft clamping limit of about 750 mA, the difference signal is used to reduce the gate voltage of the turn-off driver DMOS and thus the gate current of the IGBT. The feedback current is typically applied through 600W transient voltage suppressor (TVS) diodes in parallel to capacitors in the 100 pF range and a few additional resistors. A Monte Carlo simulation of a real-life model (not considering the variation of the breakdown voltage of the TVS) for the critical case of a turn-off with a gate resistance of 1.2 Ω at four times the nominal current of 2400 A/1700 V IGBTs shows that a rate-of-rise control with a median value of 4.8 V/ns ± 0.5 V/ns can be achieved at a voltage clamping level of 1630 V ± 20 V/ns, a DC link voltage of 1300 V, a DC link inductance of 100 nH and an overshoot voltage of below 25 V at the beginning of the clamping process. The control performance has been validated by measurements for a wide range of applications.

C. IGBT Turn-on Control

In a first operating mode, the ASIC provides a regulated +15 V gate-emitter voltage for the turn-on and on-state with a measured accuracy of ±450 mV over 3-sigma process variations and a temperature range of –40 °C to 150 °C by adjusting the IGBT emitter potential as a function of the total gate-drive supply voltage. The actuating DC current is limited to 2.6 ±0.2 mA to offer the option of overriding this control by external components in order to set a custom-specific gate-emitter voltage. For a total gate-drive supply voltage below about 20.5 V, the driver keeps the gate-emitter voltage constant at about –5.5 V to achieve a noise-immune off-state condition. For this operating mode, the clear-fault condition of the supply voltage monitoring provides a minimum gate-emitter voltage of about 12.6 V for turn-on and 5.15 V for turn-off. Appropriate startup circuitry and noise filtering have also been implemented. The recommended total range of the gate-drive supply

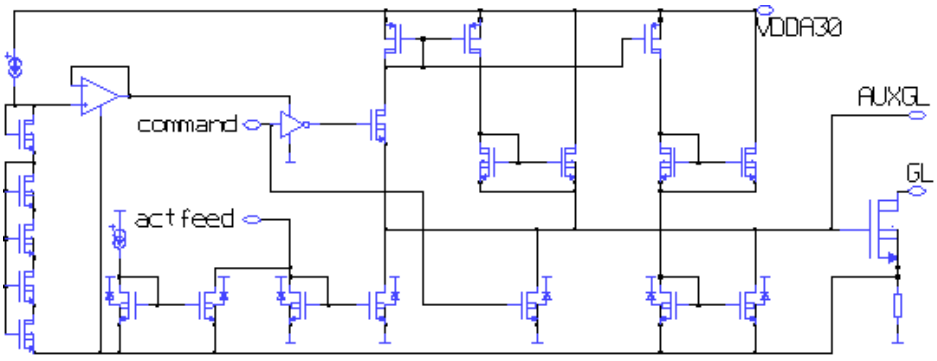

Fig. 2: IGBT turn-off control simplified schematics.

voltage is from 20.5V to 30 V. In a second operating mode known as the MOSFET mode, the ASIC also provides a turn-off voltage of 0 V. When this mode is detected by the ASIC, the clear-fault condition of the turn-on supply voltage monitor is set to about 8.5 V. Both the circuitry for monitoring the turn-off supply voltage and the regulated +15V supply voltage are then deactivated.

Optionally, the control of the turn-on gate-emitter voltage can be incorporated in a current balancing scheme for parallel-connected IGBTs.

D. Bidirectional Signal Transformer Interface

The transformer interface transmits command signals via single short pulses (with a nominal voltage level of 15 V and a duration of 185 ns) to achieve a superior command to gate delay. Differential signal processing with a highly linear input voltage of up to 40 V and soft clamping is used to increase the common-mode noise rejection. Synchronous rectification is applied to avoid large parasitic substrate currents. In the linear mode of operation, each of the two inputs has a minimum current sink capability of 220 mA such that the differential signal processing achieves a common-mode rejection of more than 110 V/ns at a coupling capacitance of 4 pF with negligible influence on delay jitter. A dedicated minimum-pulse evaluation is applied to the command signal to provide additional differential-mode noise immunity by means of a latch with a transparent period of 33 ns without introducing additional delay. Adequate damping resistors have been integrated to reduce undesired backswing voltages.

In case of a collision, the fault signal dominates both the command signal and noise by means of a longer pulse duration of 950 ns at a current level of 260 mA. This event is validated on the primary side when a current level of 40 mA is exceeded for a minimum time of 400 ns (in addition to any commands sent). This condition is identified by comparing the on-state drain-source voltage of the transformer driver n-type DMOS with the voltage across a DMOS of the same type but smaller width supplied with a correspondingly scaled reference current. To minimize the variance of these conditions, the circuitry has been compensated for temperature and process variations.

To achieve high common-mode rejection for the command signal, the circuitry for the fault signal channel is also designed to be fully symmetrical. This also allows two separate fault signals to be implemented. However, single-ended fault signal processing has currently been implemented on the primary side, as it achieves sufficient noise immunity at the cost of an increased delay jitter of the fault signal.

A superior noise immunity > 50 V/ns has been experimentally verified for both command and fault signals for a repeatedly applied offset voltage swing of up to 3300 V with a coupling capacitance of 4 pF.

This asynchronous fault transfer method also allows the special timing requirements of high-power converters to be managed, since any fault condition will be available on the primary side within 1 µs. A preferred fault-management mode thus reports the fault event prior to turn-off of the relevant IGBTs. The delay to shutdown is adjustable at the ASIC in the microsecond range and can also be set to infinity or zero.

III. APPLICATIONS

The new chipset serves as the core platform to implement a next-generation series of IGBT gate drivers.

Figure 3 shows a dual-channel gate driver core with a signal transformer interface and a driving capability of 8 A / 1 W, +15 V / -10 V with fully integrated gate drive and DC-DC converter output stages. The typical delay time is 88 ns. Their compactness, easy scaling up to seven channels and low cost make these drivers an optimized solution for driving IGBTs up to 1700 V and 225 A. Typical applications include half-bridge control of 1700 V / 150 A IGBTs at switching frequencies up to 25 kHz and 600 V / 50 A IGBTs at switching frequencies up to 85 kHz.

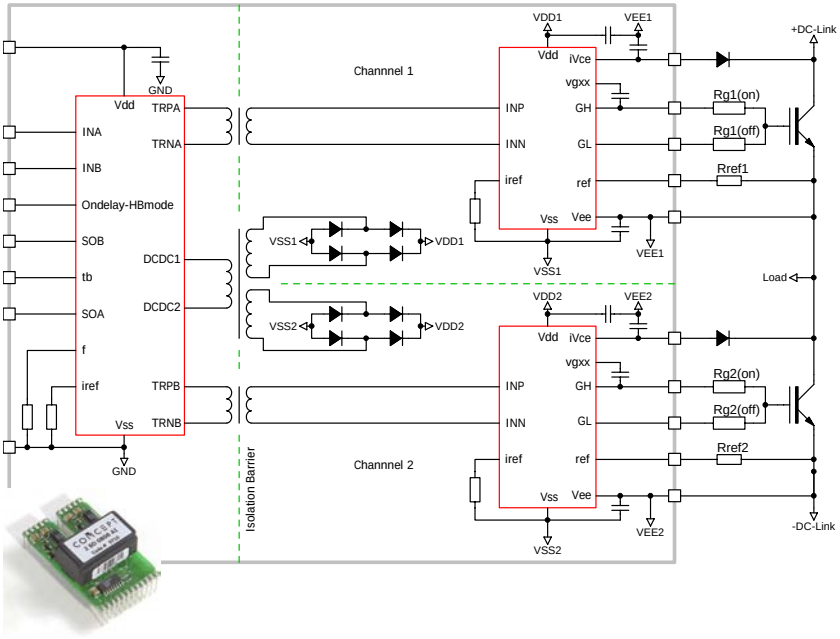

Fig. 3: Full schematics of a highly integrated dual 8 A / 1 W gate driver core.

Figure 4 shows a complete 25 A / 6 W driver with external DMOS, fiber optic interfaces and turn-off closed-loop control for IGBTs up to 3300 V. The overall component count is reduced by more than 60 % compared to the previous chipset [9].

Figure 5 shows a planar transformer gate driver core with a measured driving capability of 12 A / 12 W or 20 W at switching frequencies of 250 kHz or 120 kHz respectively at an ambient temperature of 85 °C and a junction temperature of 130 °C, a delay time below 100 ns with a peak-to-peak jitter below 2 ns. (500k acquisitions, 1 hour.)

Moreover, the ASICs are qualified to operate at junction temperatures up to 175 °C.

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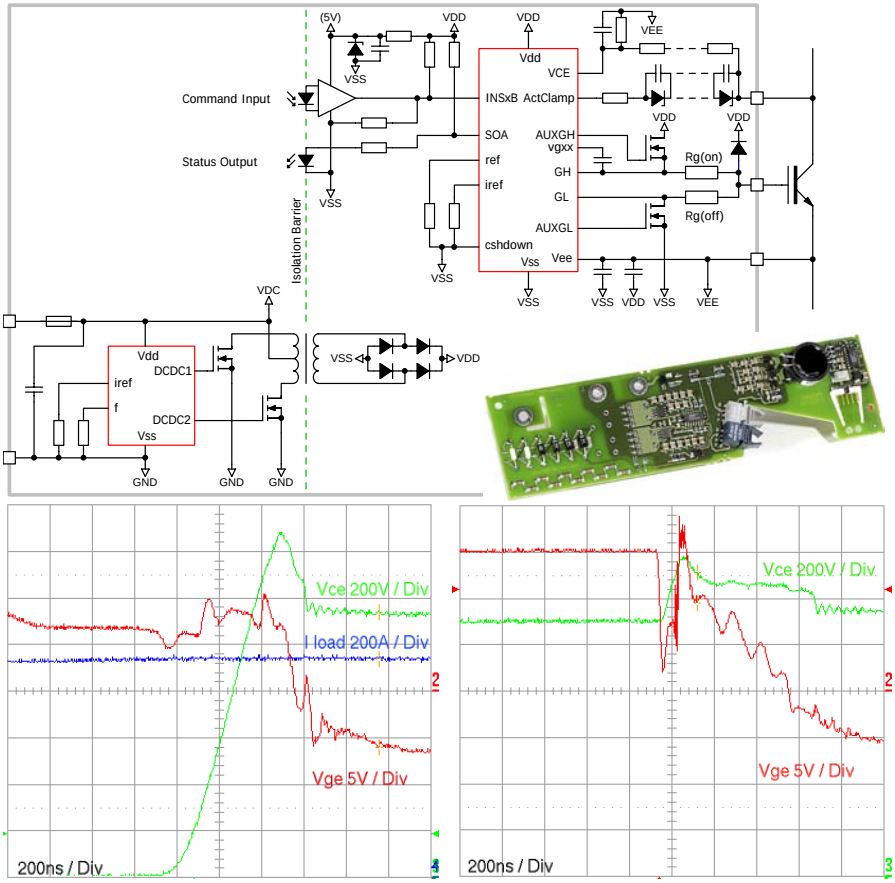

Fig. 4: Complete 25 A / 6 W gate driver for IGBTs up to 3300 V. Full schematics and implementation (top). Turn-off control of an eupec FS450R17KE3 1700 V IGBT at twice the nominal collector current (left) and at short-circuit (right).

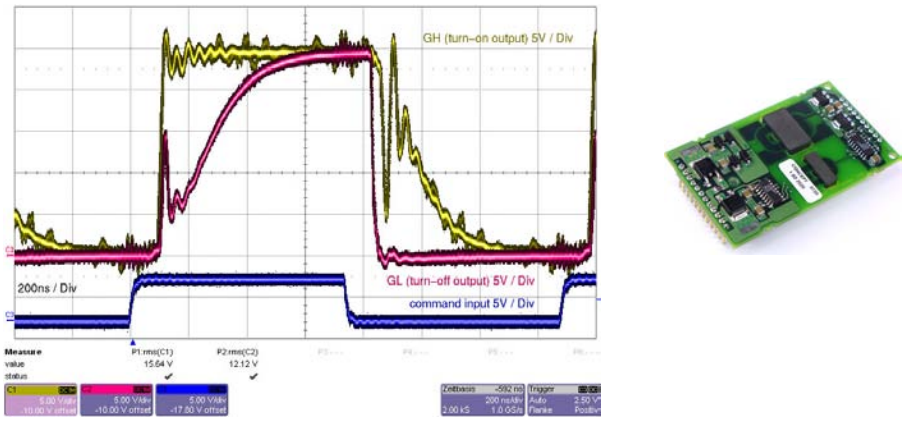

Fig. 5: Planar transformer 12 A / 12 W / 250 kHz single gate driver core. Command and output signals (persistent display to show delay jitter) at a capacitive load of 160nF via 2 Ohm and 2.2 Ohm at outputs GH and GL respectively.

REFERENCES

[1] K. Ishikawa, K. Suda, M. Sasaki and H. Miyazaki, "A 600V driver IC with new short protection in hybrid electric vehicle IGBT inverter system, " Proc. ISPSD 2005

[2] C. Kuratli, Q. Huang, A. Biber, "Implementation of high peak-current IGBT gate drive circuits in VLSI compatible BiCMOS technology," IEEE Journal of Solid-State Circuits, vol. 31, Issue 7, July 1996

[3] R. Herzer, S. Pawel, J. Lehmann, "IGBT driver chipset for high power applications," Proc. ISPSD 2002

[4] S. Pawel, J. Lehmann, R. Herzer, M. Netzel, "High power four channel IGBT driver IC," Proc. ICCDCS 2002

[5] C. Gerster, P. Hofer, N. Karrer, "Gate-control strategies for snubberless operation of series-connected IGBTs," Proc. PESC 1996

[6] K. Ishii, H. Mastumoto, M. Takeda, A. Kawakami, T. Yamada, "A high voltage intelligent power module (HVIPM) with a high performance gate driver," Proc. ISPSD 1998

[7] A. Lindberg, W. Belwon, P. Oom, "MACS ICON – IGBT based propulsion systems," Proc. EPE 1997

[8] T. Yamazaki, Y. Seki, Y. Hoshi, N. Kumagai, "The IGBT with monolithic overvoltage protection circuit," Proc. ISPSD 1993

[9] H. Rüedi and P. Köhli: "The SCALE IGBT driver: a new scalable, compact, all-purpose, low cost, easy to use driver for IGBTs," Proc. PCIM Europe 1998