# 1700V Fully Coreless Gate Driver with Rugged Signal Interface and Switching-Independent Power Supply

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***Abstract* – This paper describes development and implementation of gate drive ICs that rely exclusively on external coreless transformers. Both, signal and continuous power are transferred via coreless transformers. The newly developed "double pulse" signal transmission scheme facilitates save switching under voltage transients higher than 95 V/ns. Reliability of the planar insulation on the printed circuit board is found to be as good as for conventional ring core molding, or better. Dedicated layer buildup and material selection prevents insulation failure due to formation of conductive anodic filaments.**

## I. INTRODUCTION

Recently, alternative approaches to high voltage (HV) insulation for IGBT gate drivers have been demonstrated. High voltage insulation is based on wireless signal transmission [1], piezoelectric elements [2] as well as coreless transformers in these approaches. Both monolithically integrated coreless transformers [3] and hybrid integration on printed circuit board (PCB) level [4] are used. The elimination of the ferrite core is attractive especially because of easy automated manufacturing, reproducibility, low-profile designs and inherent cost benefits. However, most existing solutions lack certain requirements for high performance gate drivers. Most important among them are: energy transfer, delay times significantly below one microsecond, and high reproducibility of the delay time.

Wireless systems will see much improvement in the future but at the moment they are leading to high delay times because of signal demodulation. Fully integrated coreless transformers are present on the market already in the form of a proprietary technology [5]. The concept of resonant coreless gate drivers has been given great attention. However, the resonant topology suffers from the fact that the delay time is inversely proportional to the carrier frequency. High carrier frequency in the tens of megahertz leads to a drastic increase in power dissipation. The systematic delay time jitter is roughly one half of the carrier period which might easily be a factor of ten too large for high performance gate drivers.

A non-resonant coreless gate driver with resonant power transfer is therefore developed with low delay time and jitter. The integrated circuits are designed for open foundry CMOS processes.

## II. SYSTEM OVERVIEW

The gate drive circuit as shown in Fig. 1 is built around a primary and a secondary ASIC (application specific integrated circuit). The ASICs contain all integrated circuitry necessary for implementing the two main functions of a gate driver: First, to transmit signals between primary and secondary side, and second, to provide insulation and power supply for the secondary side.

There are chip-external coreless transformers on the PCB between primary and secondary side. These coreless transformers consist of spiral windings that are stacked on top of each other and that are separated by the PCB insulation material. No magnetic flux guidance, such as a ferrite core, is used.

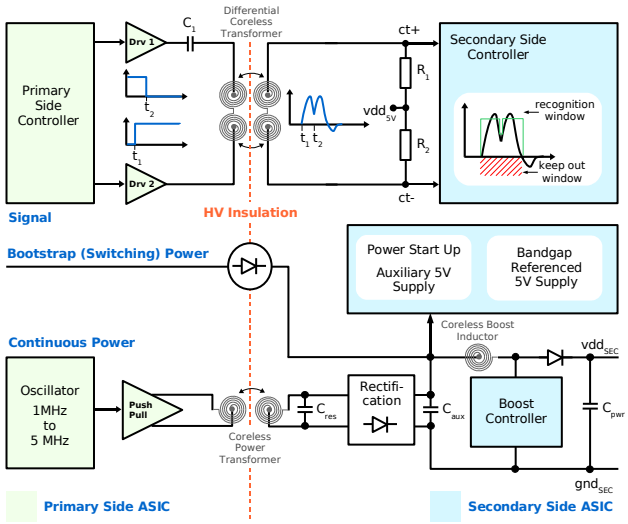


Fig. 1. Block diagram of the coreless gate drive system

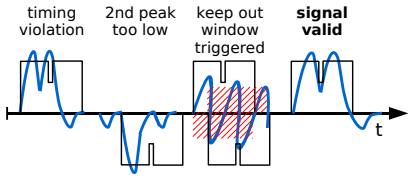


Fig. 2. Filtering of invalid input signals (functional diagram)

### *A. Signal Path*

A user-generated input signal entering the primary side controller in Fig. 1 is translated into mutually delayed switching edges and fed onto the driver stages Drv 1 and Drv 2. Both drivers are connected to a differential pair of coreless inductors in series with a high pass capacitor $C_1$. Each of the switching edges leads to current through $C_1$ and the differential coreless inductors. At the secondary side there is a resulting current due to the magnetic coupling between the coreless inductor pairs. This current flows through the series connection of the resistors $R_1$ and $R_2$, such that there is a voltage at the input of the secondary side controller. The voltage between nodes ct+ and ct- is a differential signal relative to the midpoint potential $vdd_{5V}$.

$Vdd_{5V}$ defines the DC bias point of the differential input voltage which would otherwise be completely floating.

The differential input voltage is compared to a predefined (adjustable) recognition window inside the secondary side controller. A new window is triggered at every *first* positive or negative edge of the input voltage waveform to guarantee constant delay times for signal recognition regardless of the preceding input waveform (Fig. 2). If the input voltage waveform fails to comply with the recognition window or if it enters a second "keep out" window, then the current signal edge is discarded and a new recognition attempt is started at the

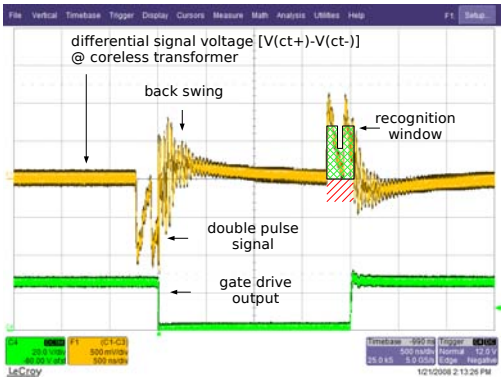


Fig. 3. Double pulse signal transmission at 250kHz

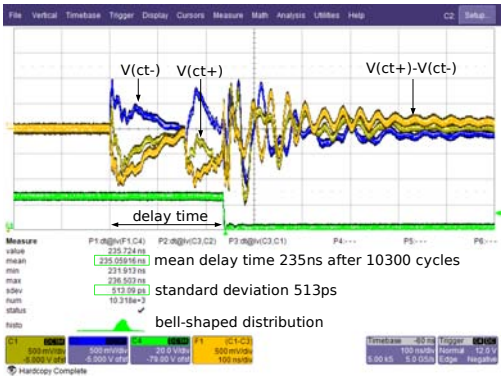


Fig. 4. Delay time distribution and jitter without external disturbance

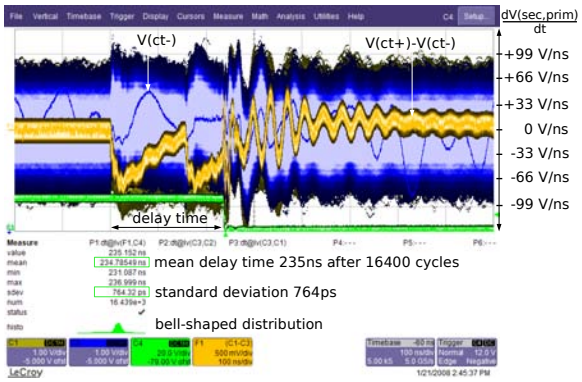


Fig. 5. Delay time distribution and jitter with common mode disturbance equal to +/-95 V/ns between primary and secondary side; random-noise-shaped dV(sec,prim)/dt

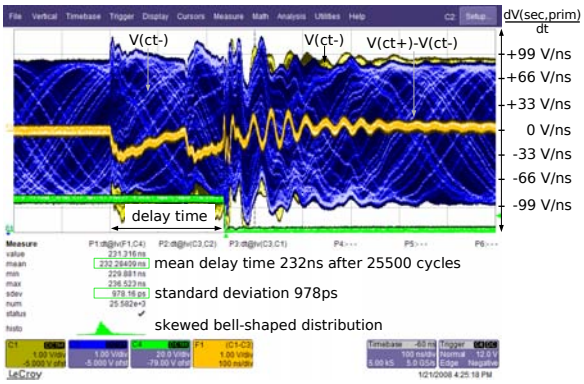


Fig. 6. Delay time distribution and jitter with common mode disturbance equal to +/-95 V/ns between primary and secondary side; sine-shaped dV(sec,prim)/dt at 1.8MHz

next rising or falling edge. The interface is thus insensitive to oscillating waveforms coupling into the signal path from the nearby IGBT or MOS power plane. The differential nature of the input voltage respective to the bias point also makes it possible to detect signals correctly that are superimposed by common mode disturbance. One important example of such disturbance is the voltage transient (dv/dt) at every IGBT or MOS switching transition where the secondary side ground potential $gnd_{SEC}$ typically changes between the positive and the negative DC link potential.

So far, all circuit blocks have been using 5V components to enhance speed and precision. For the gate drive output, however, the signal is level-shifted from 5V to +15V / -10V bipolar output voltage. The integrated level shifter limits the gate voltage swing across the external CMOS output stage to less than 15V for both the nMOS and the pMOS transistor to avoid gate degradation.

### *B. Power Supply Branch*

Secondary side power is transferred by two independent paths. The repetitive switching power needed to deliver the required gate charge to the IGBT or MOSFET is refreshed by a conventional bootstrap circuit.

A second power path has been implemented to supply continuous power and thus overcome the duty cycle limitation of the bootstrap supply alone. The switching-independent power is transferred by a known resonant coreless transformer [6] [7].

Both bootstrap supply and continuous power supply refill the charge reservoir $C_{AUX}$. The voltage across $C_{AUX}$ is directly fed into the secondary side IC where a power startup block monitors the correct sequencing of internal and chip-external supply voltages. At first a very robust auxiliary 5V supply (that is sure to start up under all operating conditions) is delivering power to the internal bandgap references and the main 5V low dropout series regulator (LDO). With the stable 5V supply provided by this LDO, the boost controller is started which delivers 25V to node $vdd_{SEC}$ for the bipolar +15V / -10V gate drive output. The boost controller applies pulse skipping at a fixed frequency. Operation is always maintained to be in discontinuous conduction mode (DCM). No shunt resistor is needed between the internal 1.3A, 40V, 3$\Omega$ switch and ground node $gnd_{SEC}$. The current is measured in every cycle by monitoring the drain source voltage of the boost switch against a temperature-compensated and process-tracking internal reference. The pulse-by-pulse current limiting can be configured to react either at a given current, after a given on-time of the boost switch or following a curve of current derating versus temperature for the internal boost switch.

## III. MEASUREMENTS

The primary and secondary ASIC (Fig. 8) were manufactured in a double metal, foundry CMOS process with 0.8$\mu$m feature size, 5V to 50V transistors, and double well insulation.

### *A. Signal Path*

Fig. 3 shows a typical switching waveform of the coreless gate drive system. The resistors $R_1$ and $R_2$ were chosen to be 22$\Omega$ each. The total coupling capacitance $C_{prim\text{-}sec}$ across the coreless signal transformer was measured to be 2.75pF. At 250kHz switching frequency, the power dissipation of the signal channel was 360mW.

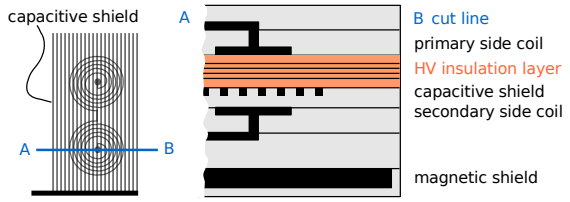


Fig. 7. Coreless signal transformer cross section (not to scale), 8-layer PCB, coupling capacitance $C_{prim\text{-}sec}$ with capacitive shield 2.75pF (9.4pF without shield), 100$\mu$m copper magnetic shield

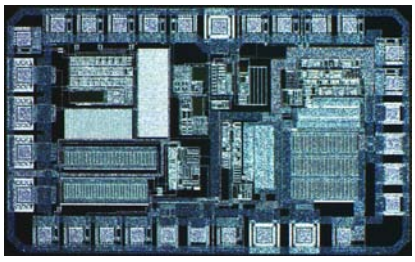

Fig. 8. Secondary side ASIC (2.8mm x 1.7mm)

The measurement of the delay time distribution over 10300 cycles is shown in Fig. 4. No systematic jitter is present, due to the asynchronous signal processing. The five sigma spread of the driver's delay time distribution is less than 2.6ns at 235ns mean delay time.

A signal generator has been connected between primary side ground and secondary side node $vdd_{5V}$ for the measurement in Fig. 5. This configuration acts to stimulate the effect of arbitrarily high change rates dV(sec, prim)/dt of the primary to secondary side voltage over time. Since $R_1$ and $R_2$ are in parallel (//) for the common mode voltage V($vdd_{5V}$) the relation between dV(sec, prim)/dt and common mode voltage at node $vdd_{5V}$ is:

$$\left.\frac{dV(sec,\ prim)}{dt}\right|_{mean} = \frac{\Delta V(vdd_{5V})}{C_{prim\text{-}sec} \cdot R_1 // R_2} \qquad (1)$$

With the given values one volt change in V($vdd_{5V}$) equates to the effect of 33V/ns for dV(sec, prim)/dt.

The common mode waveform applied in Fig. 5 was pseudo-random noise with a maximal height of +/-2.9V (+/-96V/ns). Only a very moderate increase of the five sigma spread in delay time was observed. The bell-shaped distribution shows no systematic effect of the disturbance on signal transmission.

Fig. 6 shows a measurement equal to that in Fig. 5 but with a sinusoidal disturbance voltage. The frequency of 1.8MHz was chosen to interfere in a worst case manner with the double pulse signal. Systematic influence on the delay time can be seen by the skewed distribution of measurement values with a distinct right-hand tail. The quantitative effect, however, remains very small with a formal standard deviation below 1ns.

The coreless drive system has been successfully tested in a 1.7kV switching IGBT environment at a DC link voltage of 1kV. Also, dV(sec, prim)/dt testing has been performed where an auxiliary gate driver was controlling the IGBT and where the coreless drive system was sharing primary side and secondary side ground with the auxiliary gate driver. Arbitrary timing positions of the dV(sec, prim)/dt phase relative to the double pulse signal were thus attainable. Coreless signal transmission was found to be 100% operational at all timing positions during dV(sec, prim)/dt slopes up to +/-98V/ns – the highest dv/dt that could be produced in the test setup. During these measurements, a strongly inhomogeneous magnetic stray field of approx. 91mT was applied perpendicular to the PCB. The rate of change for this magnetic field was 13mT/us. A 100$\mu$m thick copper layer covering the coreless

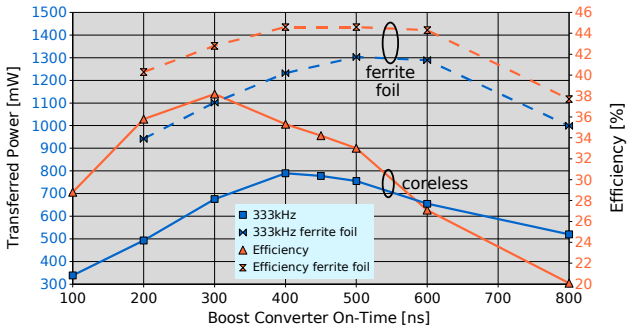


Fig. 9. Continuous power output after 333kHz boost stage to 25V (transformer area 78mm$^2$, 15V primary side input, 3.7MHz at coreless transformer, coreless boost inductor 4.6$\mu$H, area 78mm$^2$)

signal transformer acts as a magnetic eddy current shield (see Fig. 7). At a frequency of 1MHz its shielding efficiency is already 93%. The lowest relevant frequency component of the double pulse signal is significantly higher than 1MHz at roughly 1.6MHz.

It has been specifically looked for skipped pulses, where the signal transmission would have been inhibited by the aforementioned disturbances. No skipped pulses occurred during the measurements.

### *B. Continuous Power Supply*

Efficiency and total transferable power have been measured for a continuous power path as depicted in Fig. 1. Fig. 9 shows the results of two measurement series for the whole chain from primary side push pull driver to secondary side output $vdd_{SEC}$. In the first series, all inductances were coreless planar windings. In the second series, the planar resonant transformer on the PCB was equipped with a polymer-ferrite foil for magnetic flux concentration. The boost inductor remained coreless in both series.

Usable power of 750mW is provided by the fully coreless power branch over a wide parameter space. The boost converter efficiency is best at low duty cycles due to the relatively high on-resistance of the chip-internal boost switch and the low value of the coreless boost inductor; both leading to elevated conduction losses.

Using a ferrite foil for flux concentration in the planar resonant transformer increases the usable power by 65% with a 25% increase of the efficiency at maximum power. The coreless boost converter showed efficiencies above 90% in both series.

The transferred power of 750mW in the fully coreless case is more than sufficient to supply standby power to the gate driver's secondary side. The main switching power used to charge the IGBT or MOSFET gate is transferred by the parallel bootstrap power branch.

## IV. RELIABILITY

### *A. Accelerated Aging*

A sample group of PCB HV insulation structures was tested against a control group of tried and tested 1.7kV transformers made with resin-molded ring cores. The criterion for insulation quality was chosen to be partial discharge extinction voltage, because this allows repetitive non-destructive testing. Partial discharge inception was forced in each sample and the extinction voltage measured versus thermal cycles between -40°C and 125°C. The results are shown in Fig. 10 normalized to the initial mean value of the control group.

The optimized PCB HV insulation layer of the coreless transformers shows very stable aging behavior. This is even more significant as the control group consisted of series production parts with a known mean time to failure (MTTF) well above ten million hours.

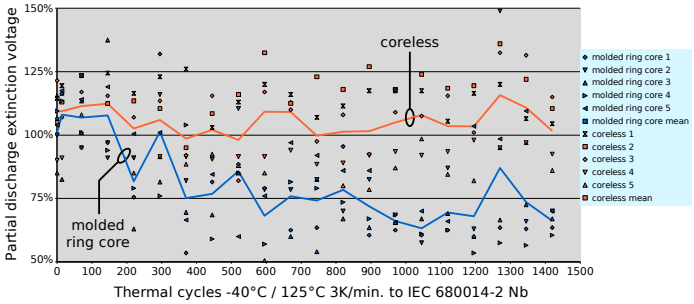


Fig. 10. Partial discharge extinction voltage vs. thermal cycling, extinction voltages normalized to initial value of molded ring core group

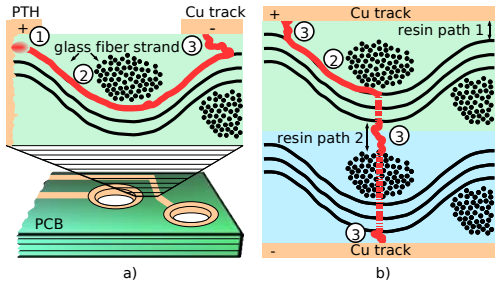


Fig. 11. Schematic CAF paths, a) lateral CAF, b) vertical CAF

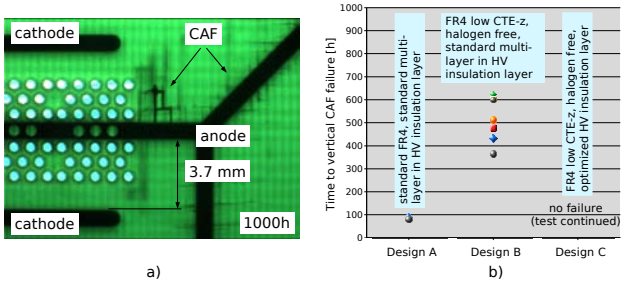


Fig. 12. Temperature-humidity-bias test at 85°C/85% rel. hum, 1.5kV DC
a) Lateral CAF formation in standard FR4, cascaded holes stop filament growth and retain much of the original mechanical strength of the PCB
b) Vertical CAF in HV insulation layer vs. material and layer buildup

### *B. Conductive Anodic Filament Formation*

Fiber-reinforced resin materials, and particularly FR4-type glass-epoxy systems, are prone to the growth of conductive anodic filaments (CAF). Two exemplary cases are illustrated in Fig. 11. Since the early studies it is clear that CAF problems are more severe under high voltage stress and humidity [8] [9]. CAF propagation is commonly seen as a two-step process [10] [11], where in a first step ① the bond between the epoxy resin and the glass fibers is weakened. This can be due to mechanical damage as in case of a drill hole for a plated through hole (PTH) and/or due to debonding of silane bridges between glass fiber and epoxy resin [12]. The latter effect is strongly influenced by material selection, surface treatment, flux chemistry, and thermal stress. Especially the discrepancy in the coefficient of thermal expansion (CTE) between glass fibers and resin leads to high shear forces at the glass-resin bond under temperature cycling stress.

The CAF then propagates along a weakened glass fiber surface in step ②. The filament itself consists of copper salts that are dissolved at the copper anode and deposited along the propagation front. Both electrical potential and pH value of the aqueous copper salt solution influence the complex chemical equilibrium process [10].

A third step is introduced here into the qualitative CAF model to cope with multi layer PCBs under high voltage stress. Step ③ comprises the propagation of the filament through resin paths towards the cathode. The underlying process is not clear at the moment. It can be hypothesized that the propagation through solid resin is following structural weaknesses, cracks and micro-fissures. Partial discharge corrosion in the high-field region at the cathode-side end of the CAF might also be contributing to resin erosion.

Detailed CAF tests have been performed to ensure reliability of the HV insulation layer on the PCB (Fig. 12b). After 75 temperature cycles between -45°C and 120°C, the different designs were exposed to a temperature-humidity-bias (THB) test at 85°C and 85% rel. humidity. The DC bias voltage was much higher than in conventional tests with a constant value of 1500V.

From Fig. 11 it is clear that there are distinguished countermeasures necessary against lateral CAF and vertical CAF. Lateral CAF can be stopped by overlapping arrays of non-plated through holes as shown in Fig. 12a. Slotting has the same effect but it further reduces the mechanical strength of the PCB.

Vertical CAF can be suppressed by carefully optimizing the layer buildup of the HV insulation. Especially the implementation of long accumulated resin paths and high resin excess does contribute. The resin excess of copper-clad FR4 sheets (resin path 1 in Fig. 11b) is reduced by the copper foil surface roughness (deliberately increased by etching to achieve good bonding between copper and resin).

Advanced FR4 material with low z-axis CTE and halogen free flame retardant was found to be a major step towards CAF resistance. The chemistry of the curing and cross-linking agent without the use of dicyandiamide (DICY) also plays an important role [10] [12].

With design C in Fig. 12b, a CAF resistant platform has been developed that is easy to manufacture in standard PCB processes.

## V. CONCLUSION

The fully coreless HV gate drive system has been developed and analyzed. Both a high signal transmission speed and robustness against real-world spurious signals in IGBT and MOSFET applications was achieved. HV insulation on the PCB is found to promise reliable operation for the 1.7kV class and beyond, considering aging and CAF. Material selection and layer buildup are pivotal to CAF resistance.

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